Revision of Various Square-Root algorithms for efficient VLSI Signal processing applications

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Abstract: With initiation of VLSI signal processing concept, Very large scale integration technique becomes more powerful in the field of signal processing. Now a day, many of the researchers are now trying to integrate the VLSI technique with the signal processing theory. Hence analyzing device, designing and manipulating the performance from circuit & system level perspectives becoming a vital task and challenging too. The study of various diverse algorithms that are used for square root circuit design is the central focus of this paper. In particular, we provide a comprehensive survey of different designing techniques, complementing the limits of existing reviews in the literature. The survey covers introduction to VLSI technologies, motivation towards the work, various square root algorithms with their limitations etc. This paper can be seen as a foremost stab to present a state-of-the-art impression of the research work carried in the field VLSI signal processing applications.

Keywords - FPGA, *Newton method*, *NR algorithm*, *Rough estimation*, *Restoring*, *Square root algorithms*, *VLSI Signal Processing*, *VHDL*

I. Introduction

Verifying the integrity in the VLSI technique and detecting the traces of tampering without using any protecting pre-extracted or pre-embedded information in signal processing have become an important and hot research in the field of VLSI signal processing. The popularity of this field and the rapid growth in papers published in recent years has put considerable need on creating a complete paper showing existing methods. The present paper represents a comprehensive list of references on design of square root circuit by using various diverse algorithms. Though there are some other published surveys, many of existing designing techniques for VLSI signal processing applications are uncited and remain unidentified. In this article we do not contemplate to go into niceties of particular methods or describe results of comparative experiments. This work also does not contain articles from popular press or papers only giving general information about various square root circuit design techniques. We will try to directly jump into the core topic of the paper. We hope that this work will help the researchers in the specific domain to find new research problems and solutions. An attempt has been made to make this paper complete by listing most of the existing references. The authors have tried to blueprint a thorough classification group and fit the presented references into this classification. To the superlative knowledge of the authors, this bibliography appears to be the most complete published source of references on design of square root circuit by using various algorithms.

II. Motivation Towards Work

We selected this topic to do the research work on this because; now a days the era of VLSI signal processing involves in designing various circuits .These circuits intended for various signal processing applications. The applications may be squaring, square root etc. Square root is an important arithmetic operation, so this circuit is designed by means of various algorithms. This study involves in explaining and analyzing various square root algorithms for efficient VLSI signal processing applications. It will help all the researchers to develop, analyze and integrate various circuits intended for specific applications.

III. Various Square-Root Algorithms

There are several different methods for determining the square root of a number. Some giving a rough approximation, others giving an exact value. Some of the methods are given below. There have been published several surveys on designing square root circuit using various square root algorithms. Despite these existing surveys, most of the existing methods for designing circuits are uncited and remain unidentified. Our huge effort in this paper was to include the existing references that directly deal with design of square root circuit.

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A. Using Prime Factorization

In this method [1] a number's factors are used to find a number's square root. The answer can be an exact numerical number or a close estimate depending on the number. A number's factors are any set of other numbers that multiply together to make it. The steps of this method are illustrated below.

Step 1- Divide your number into perfect square factors.

Step 2- Take the square roots of your perfect square factors.

Step 3- If your number doesn't factor perfectly, reduce your answer to simplest terms.

Step 4- If needed, estimate.

Step 5- Alternatively, reduce your number to its lowest common factors as your first step.

B Long division Method

This is a method of finding the square root which uses division method [2]. An exact result can be obtained by using this algorithm. The steps of this method are given below.

Step 1-Separate the number's digits into pairs.

Step 2-Find the largest integer n whose square is lesser than or equal to the leftmost number (or pair).

Step 3-Subtract the number you just calculated from the leftmost pair.

Step 4- Drop down the next pair.

Step 5- Fill in the blank spaces in the right quadrant.

Step 6- Subtract the number you just calculated from the current number on the left.

Step 7- Repeat step 4.

Step 9- Repeat step 5 and 6.

Step 10- To continue to calculate digits, drop a pair of zeros on the left, and repeat steps 4, 5 and 6.

C. Newton Method

The Newton's method [3] is one of the methods for extracting the square root of a number. This is also known as Newton-Raphson method for finding square root. Newton's method provides a better approximation to the square roots of a real valued number. But in this method derivatives are required to be calculated directly which needs the analytical expansion for the derivative. This calculation is expensive to evaluate and could not be easily obtained. The steps of this method are given below.

Step 1-Start with an initial rough guess that is \boldsymbol{x}_0 .

Step 2-Starting at the point x_0 on the x-axis, go up to the curve, hitting it at the point $(x_0, f(x_0))$.

Step 3-Slide down the tangent line to the curve at $(x_0, f(x_0))$ and take the point where this tangent line hits the x-axis as the improved estimate for the desired x-value. Name this value x_1 .

Step 4-The tangent line has slope $f'(x_0)$ and passes through the points $(x_0,f(x_0))$ and $(x_{1,0})$. This gives the equation:

$$x_1 = x_0 - \frac{f(x_0)}{f'(x_0)} \tag{1}$$

 $x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)}$ (2)

Step 5- Replace x_0 by x_1 and repeat as often as needed. It will produce a sequence of guesses x_0 , x_1 , x_2 , and these will get closer to a root.

D. Digit by digit Method

This is a method [4] of square root calculation in which each digit of the square root can be found in a sequence. This method is easier for manual calculation as compared to other methods. This algorithm can be implemented for any base and depends on the base chosen. By using this method we can check whether a number is a squared number or not. This method provides almost correct result for the square root but the calculation time is more as compared to other methods.

E. Babylonian Method

The Babylonian method [5] is known to be the first method developed for square root calculation of a number. It provides the approximate value of the square root. The basic steps of Babylonian method are given below.

Step 1-Determine the overestimate to the square root of the given number.

Step 2-Determine the underestimate to the same number

Step 3-Take the average of the numbers obtained from step 1 and step 2.

The average obtained is supposed to provide the result. This method is having some limitations. Some of them are given here. 0To determine the result, this method needs the arithmetic and geometric means. This

shows that the squared root is always overestimate to the square root. This method can be implemented for the non-negative real valued number only. The result obtained is only the approximated value not the exact one. During the calculation time some computational error arises.

F. Rough Estimation Method

This is a method [6] of square root calculation that can be done by pen and paper only. It provides an estimated value of the result. A real valued non-negative number's square root can be determined easily by using this Rough estimated method. There are some limitations in this method. Like an initial seed value is needed for calculation and geometric mean is also required for square root extraction.

G. Restoring Method

Restoring algorithm [7] for square root calculation is a trial and error method of approach. In this method the remainder bit is restored for further calculation. The steps of this method are given below.

Step 1-Put x in register A, d in register B, 0 in register P, and

Perform *n* divide steps (*n* is the quotient word length)

Step 2-Shift the register pair (P, A) one bit left

Step 3- Subtract the contents of B from P, put the result back in P

Step 4- If the result is negative, set the low-order bit of A to 0 otherwise to 0

Step 5- If the result is negative, restore the old value of P by adding the contents of B back in P. After n cycles, A will contain the quotient, P will contain the remainder

In this algorithm both the divisor and dividend are required to be of same number of bits. If mismatch occurs then the divisor is padded with required number of zeros in its left to make them of equal bit length.

Some of the limitations of restoring algorithm are given. This method requires extra number of steps and uses multipliers. Close attention to the timing of various operations in restoring square root method is essential.

H. Non-restoring Method

Due to various advantages as compared to other square root extraction methods the non-restoring method [8] is preferred nowa days with wide implementations. It requires only limited number of arithmetic operations due to which the calculation time is reduced and calculation becomes simple and easy. So no more computational complexity arises like other methods. Here the remainder bit does not required to be stored like restoring method. This can be implemented with fewest number of hardware resources and it is best suitable for FPGA implementation. The hardware implementation is very simple. The steps of the non-restoring method are described below. This algorithm can also be used for various design of divider architectures for efficient VLSI Signal processing applications as proposed by A. sahu and Siba K.Panda [9].Again using this admired method Siba K. Panda *et al.* designed an efficient pipelined square root architecture [10] for the multiplicity of VLSI signal processing applications.

Assume that there is an accumulator and MQ register, each of k-bits. MQ_0 , (LSB of MQ) bit gives the quotient, which is saved after a subtraction or addition. X register has (2k-1) bit for dividend and Y has the k-bit divisor and a sign-bit S shows the sign.

Step 1-Load (upper half k-1 bits of the dividend X) into accumulator k-bit A and load dividend X (lower half bits into the lower k bits at quotient register MQ

Step 2-Reset sign S = 0

Step 3-Subtract the k bits divisor Y from S-A (1+ k) bits and assign MQ₀ as per S

Step 4-If sign of A, S = 0, shift register pair A-MQ left and subtract the k bits divisor Y from S-A (1+ k bits); else if sign of A, S = 1, shift register pair A-MQ left and add the divisor Y into S-A (1 + k bits)

Step 5-Assign MQ₀ as per S

Step 6-Repeat step 3 again till the total number of operations is k.

Step 7-If at the last step, the sign of A in S = 1, then add Y into S-A to leave the correct remainder into A and also assign MQ₀ as per S, else do nothing. A has the remainder and MQ has the quotient

IV. Discussions And Conclusion

To our preeminent acquaintance, this paper is the most inclusive in print source of references on various square root algorithms for designing square root circuits anticipated for VLSI signal processing applications .We deem that it can help researchers to understand, implement as well as develop a hybrid algorithm ideas and to help the VLSI signal processing image processing society to find innovative research challenges. Without any hesitation, modern years have brought a momentous improvement in the field of VLSI signal processing prospective by designing and implementing various arithmetic and logical circuits for

processors. In spite of this enhancement, perfection and prominent methods, at rest a lot of limitations and imperfections are found in the existing methods. So researcher may able to develop and implement a hybrid square root algorithm. With this hybrid algorithm fresh, innovative high performed designs can be done at surface level. Generally, we can state that the state-of-the-art of design methods and algorithms helps in understanding a concrete knowledge for designing and implementing the various square root circuits. As an implication for the prospective future work, it can be declared that this study or revision of various square root algorithm helps in generating a common test, competent performance evaluation, design innovation and proficient implementation in an enhanced approach.

References

- [1]. B R Ambedkar, S S Bedi, A new factorization method to factorize to RSA public key encryption, IJCSI International Journal of Computer Science Issues, Vol. 8, Issue 6, No 1, November 2011
- [2]. Taek –Jen Kwon, Jeff Sondeen, Jeff Draper, Floating point division and square root using a Taylor-Series expansion algorithm, IEEE conference,2007
- [3]. Nicholas J.Higham, Newton' method for the Matrix Square Root, Mathematics of computation, April 1986
- [4]. Tole Sutikno, An efficient implementation of non-restoring square root algorithm in gate level, International association of computer science and information technology,2011
- [5]. Olga Kosheleva, Babylonian method of computing and square root : Justification based on fuzzy techniques and on computational complexity, IEEE conference ,2009
- [6]. Jaspreet kaur,nirmal Singh Grewal, Design and FPGA implementation of a novel square root evaluator based on Vedic mathematics, International Journal of Information and Computation Technology,2014
- [7]. Najib Ghatte,Shilpa Patil,Deepak Bhoir, Double precision Floating Point Square Root Computation, International Journal of Engineering Trends and Technology, July 2014
- [8]. John O'Leary, John Miriam Lesser, Janson Hicky, Mark Aagaard, Non-restoring integer square root: A case study in design by principled optimization,1994
- [9]. Siba Kumar Panda, Arati Sahu, A novel Vedic divider architecture with reduced delay for VLSI applications, International Journal of Computer Applications, June 2015
- [10]. Arpita Jena, Siba Kumar Panda, FPGA-VHDL implementation pf Pipelined Square root circuit for VLSI signal processing applications, International Journal of Computer Applications, May 2016

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